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Capacitance Scaling Based Energy Effcient FIR Filter For Digital Signal Processing

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***Abstract*— In this work, we are implementing FIR Gaussian low pass filter using DSP slice available in 28nm Kintex-7 FPGA. In order to make energy efficient filter, we are using capacitance scaling. During capacitance scaling, we observe that there is no change in clock power, logic power, signal power and DSP power. But, there is significant reduction in IOs power, leakage power and total power of FIR filter on 28nm Kintex-7 FPGA. There is approx 44.74% reduction in IOs power when FIR filter operating frequency is 5GHz, 50GHz, 500GHz and 1THz and capacitance is scale down from 25pF to 5pF. There is approx 87.65% reduction in leakage power when FIR filter operating frequency is from 500GHz to 5GHz. There is approx 99.51% reduction in leakage power when FIR filter operating frequency is from 1THz to 5GHz.**

Keywords—Digital Signal Processing, FPGA, Capacitance Scaling, Energy Effcient, Filter, DSP Slice

I. INTRODUCTION

There are 240 DSP slice is available in Kintex-7 FPGA. In the implementation of FIR Filter on Kintex-7 FPGA, we are using 7 out of 240 DSP slice. The feature of DSP slice is shown in Figure 1. In our work, we are reducing the capacitance of FIR Filter in order to make this more energy efficient one.

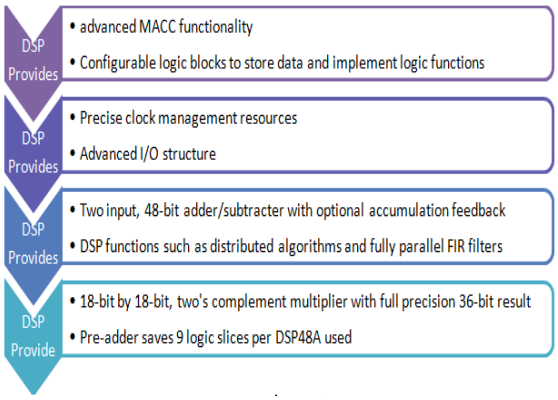

Figure1: Functionality of DSP FPGA

Capacitance is directly proportional to power dissipation as shown in Equation 1. For a fixed unit of time, power consumption is same as energy consumption. In order to make energy efficient FIR filter, we scale down capacitance to match the desired energy requirement. We are taking capacitance in range of 25pF-5pF with step size of 5pF.

$$Power \ \alpha \ Capaci\tan ce \quad \text{.....(1)}$$

A low-pass filter permit the passage of low-frequency signals and prohibits signals higher than the cutoff frequency. In digital signal processing, the impulse response of a Gaussian filter is a Gaussian function (or an approximation to it). We are operating FIR Gaussian low pass filter with 5GHz minimum operating frequency and 1THz maximum operating frequency. There are also 50 GHz and 500GHz intermediate operating frequency taken to take power reading of FIR filter.

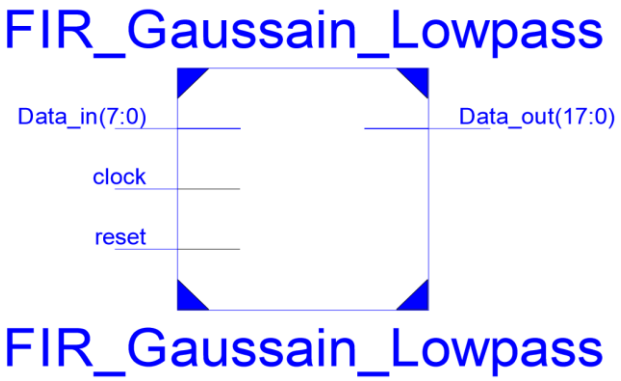

Figure2: Top Level Schematic of Gaussian Low Pass FIR Filter

In Section 2, we study and analysis different past work done in this field. In section 3, we analyze the effect of capacitance scaling in digital processing domain especially for FIR filter. In section 4, we conclude our finding and results. In section 5, we discuss what is the future scope of this research.

II. LITERATURE REVIEW

The dynamic power dissipation of digital CMOS circuit is dependent on both capacitance of payload and switching activity of circuit [2]. Clock signals are main factor behind generation of a significant portion of dynamic power in FPGAs because of high toggle device operating frequency and capacitance[3]. In particular, the values of on-board capacitance and resistance of snubber circuit has been

examined by using circuit analysis tool and field solver[4]. In order to create interconnects using memristors may also create capacitance shielding with unused routing paths. It also decreases interconnect delay [5]. Pipeline circuit and register is used to store the intermediate results and also uses the capacitance of input of different blocks[6]. Two capacitor voltages may be different due to their mismatched equivalent series resistance (ESR), their mismatched capacitance and the mismatched conducting time of the corresponding switches[7]. Low Capacitance graphene wires based graphene system application and experimentally show the potential for ultralow power electronics[8].

III. ROLE OF CAPCITANCE IN ENERGY EFFCIENT FIR FILTER

A. Power Consumption For 25pF Capacitance

Table 1: Power of Gaussian Low Pass FIR Filter for 25 pF Capacitance

	DSPs Power	IO Power	Leakage Power	Total Power
5GHz	0.104	1.359	0.132	1.651
50GHz	1.036	13.585	0.290	15.411
500GHz	10.358	135.851	1.028	152.148
1THz	20.716	271.701	1.028	303.438

In Table 1, Total power consumption of Gaussian low pass FIR filter for 25pF capacitance is 1.651W, 15.411W, 152.148W and 303.438W on 5GHz, 50GHz, 500GHz and 1 THz operating frequency respectively. Total power is a sum total of dynamic and static power. Dynamic power depends on the capacitance. Whereas static power does not directly depend on capacitance.

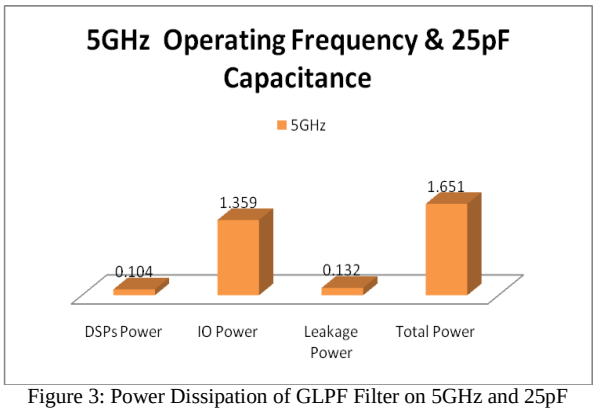

Figure 3: Power Dissipation of GLPF Filter on 5GHz and 25pF

B. Power Consumption For 20pF Capacitance

Table 2: Power of Gaussian Low Pass FIR Filter for 20 pF Capacitance

	DSPs Power	IO Power	Leakage Power	Total Power
5GHz	0.104	0.176	0.131	1.468
50GHz	1.036	11.763	0.259	13.558
500GHz	10.358	117.631	1.028	133.929
1THz	20.716	235.263	1.028	267.000

In Table 2, Leakage power consumption of Gaussian low pass FIR filter for 20pF capacitance is 0.131W, 0.259W, 1.028W and 1.028W on 5GHz, 50GHz, 500GHz and 1 THz operating frequency respectively. Leakage power depends on the temperature of device. First, change in Capacitance of FPGA affect junction temperature of device. Then, change in temperature affect leakage power of FIR Filter.

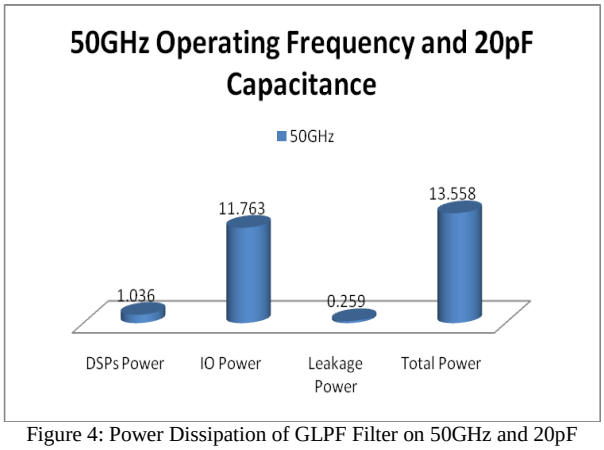

Figure 4: Power Dissipation of GLPF Filter on 50GHz and 20pF

C. Power Consumption For 15pF Capacitance

Table 3: Power of Gaussian Low Pass FIR Filter for 15 pF Capacitance

	DSPs Power	IO Power	Leakage Power	Total Power
5GHz	0.104	0.994	0.130	1.285
50GHz	1.036	9.941	0.231	11.708
500GHz	10.358	99.412	1.028	115.710
1THz	20.716	198.825	1.028	230.562

In Table 3, IO power consumption of Gaussian low pass FIR filter for 15pF capacitance is 0.994W, 9.941W, 99.412W and 198.825W on 5GHz, 50GHz, 500GHz and 1 THz operating frequency respectively. IOs power is a part of dynamic power and it depends on the selection of IO standard. In this FPGA, LVCMOs is default IO standard for FIR Filter. We can change that to SSTL, HSTL and LVDCI depend on the internal property of target design on FPGA.

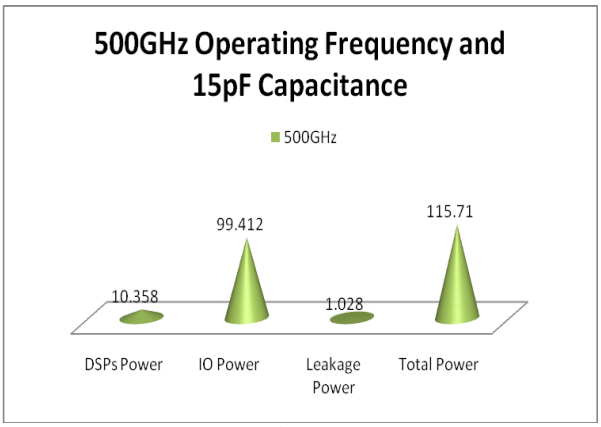

Figure 5: Power Dissipation of GLPF Filter on 500GHz and 15pF

D. Power Consumption For 10pF Capacitance

Table 4: Power of Gaussian Low Pass FIR Filter for 10 pF Capacitance

	DSPs Power	IO Power	Leakage Power	Total Power
5GHz	0.104	0.812	0.129	1.101
50GHz	1.036	8.119	0.207	9.862
500GHz	10.358	81.193	1.028	97.491
1THz	20.716	162.387	1.028	194.124

Kintex-7 FPGA provide 2 times price and performance improvement as well as 50% less power consumption compared to previous generation FPGAs. In the implementation of FIR filter on Kintex-7 FPGA, it uses 7 out of available 240 DSP slice, the power consumption by DSP slice is known as DSP power. The DSP power dissipation of FIR Filter is 0.104W, 1.219W, 12.193W, and 24.386W on 5GHz, 50GHz, 500GHz and 1 THz operating frequency respectively for 10pF capacitance as shown in Table 4 and Figure 5.

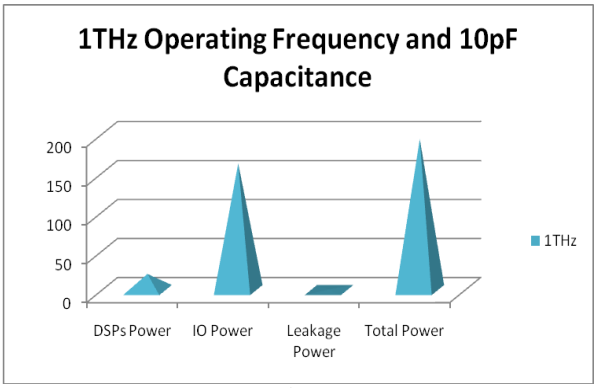

Figure 6: Power Dissipation of GLPF Filter on 1THz and 10pF

E. Power Consumption For 5pF Capacitance

Table 5: Power of Gaussian Low Pass FIR Filter for 5 pF Capacitance

	DSPs Power	IO Power	Leakage Power	Total Power
5GHz	0.104	0.751	0.127	0.918
50GHz	1.219	7.511	0.203	9.478
500GHz	12.193	75.112	1.028	93.701
1THz	24.386	150.223	1.028	186.511

There is no change in DSPs power, signal power and logic power with change in capacitance. But, IO power, leakage power and total power is affected with change in capacitance as shown in Table 1-5 .

F. Comparison of IO Power Consumption

Table 6: IO Power of Gaussian Low Pass FIR Filter

	5pF	10pF	15pF	20pF
5GHz	0.751	0.812	0.994	1.176
50GHz	7.511	8.119	9.941	11.763
500GHz	75.112	81.193	99.412	117.631
1THz	150.223	162.387	198.825	235.263

There is approx 36% reduction in IOs power when FIR filter operating frequency is 5GHz, 50GHz, 500GHz and 1THz and capacitance is scale down from 20pF to 5pF. There is approx 24.45% reduction in IOs power when FIR filter operating frequency is same as above and capacitance is scale down from 15pF to 5pF as shown in Figure 7 and Table 6.

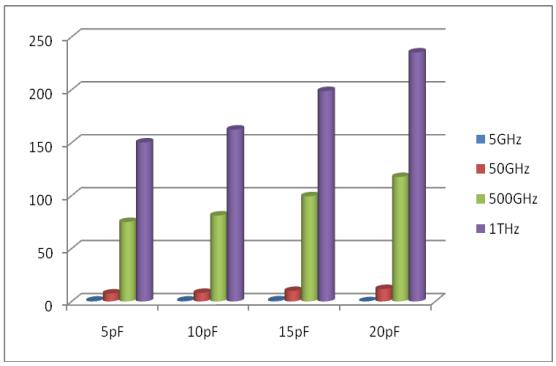

Figure 7: IO Power of Gaussian Low Pass FIR Filter

G. Comparison of Leakage Power

Table 7: Leakage Power of Gaussian Low Pass FIR Filter

	5pF	10pF	15pF	20pF
5GHz	0.127	0.129	0.130	0.131
50GHz	0.203	0.207	0.231	0.259
500GHz	1.028	1.028	1.028	1.028
1THz	1.028	1.028	1.028	1.028

There is approx 87.65% reduction in leakage power when FIR filter operating frequency is from 500GHz to 5GHz as shown in Figure 8 and Table 7. There is approx 80.25 % reduction in leakage power when FIR filter operating frequency is from 500GHz to 50GHz as shown in Figure 8 and Table 7.

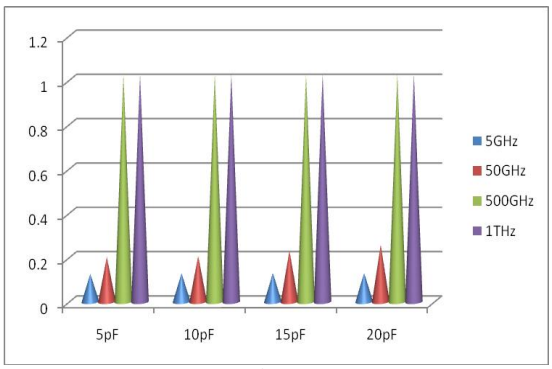

Figure 8: Leakage Power of Gaussian Low Pass FIR Filter

H. Comparison of Total Power Dissipation

Table 8: Total Power of Gaussian Low Pass FIR Filter

	5pF	10pF	15pF	20pF
5GHz	0.918	1.101	1.285	1.468
50GHz	9.478	9.862	11.708	13.558
500GHz	93.701	97.491	115.710	133.929
1THz	186.511	194.124	230.562	267.000

There is approx 99.51% reduction in leakage power when FIR filter operating frequency is from 1THz to 5GHz as shown in Figure 9 and Table 7. There is approx 30.14% reduction in leakage power when capcitance of Kintex-7 FPGA is from 20pF to 5pF as shown in Figure 8 and Table 7.

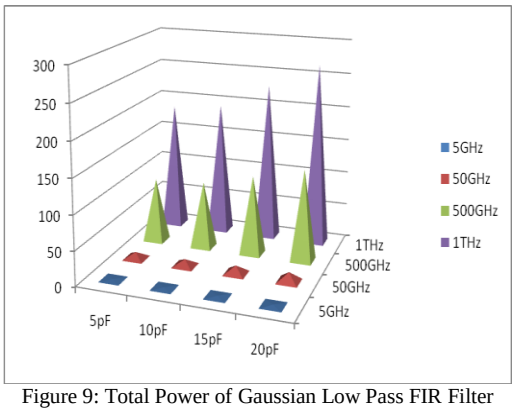

Figure 9: Total Power of Gaussian Low Pass FIR Filter

IV. CONCLUSION

There is no change in DSPs power, signal power and logic power with change in capacitance. But, IO power, leakage power and total power is affected with change in capacitance. There is approx 44.74%, 36%, 24.45% reduction in IOs power when FIR filter operating frequency is 5GHz, 50GHz, 500GHz and 1THz and capacitance is scale down from 25pF, 20pF and 15pF to 5pF respectively. There is approx 87.65%, 80.25% reduction in leakage power when FIR filter operating frequency is from 500GHz to 50GHz and 5GHz respectively. There is approx 99.51% reduction in leakage power when FIR filter operating frequency is from 1THz to 5GHz and 30.14% reduction in leakage power when capcitance of Kintex-7 FPGA is from 20pF to 5pF.

V. FUTURE SCOPE

In this work, we are implementing Filters on Kintex-7 FPGA using available 240 DSP slice. There is open scope to design other energy efficient DSP IP block like Floating-Point, Modulation, Transforms, Trig Functions, Demodulation, Video, Error Correction, Imaging and even more DSP IP block. Our Current FPGA is 28nm FPGA, there is open scope to re-implement this design on 16nm or even lower 7nm ultra scale FPGA.

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